



1 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2 Application Serial No. .... 09/665,920  
3 Filing Date ..... Sep 20, 2000  
4 Inventorship ..... Haba et al.  
5 Applicant ..... Rambus Inc.  
6 Group Art Unit ..... 2841  
7 Examiner ..... Phan, T.  
8 Attorney's Docket No. .... RB1-008US  
9 Title: Multi-Channel Memory Architecture

10 **RESPONSE TO 12/06/01 OFFICE ACTION**

11 To: Commissioner of Patents and Trademarks  
12 Washington, D.C. 20231

13 From: Daniel L. Hayes (Tel. 509-324-9256; Fax 509-323-8979)  
14 Customer No. 29150



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15 **AMENDMENTS**

16 **In the Claims**

17 Please cancel claims 9, 10, and 22.

18 Please replace remaining claim 1-8, 11-21, and 23-30 with the following,  
19 which claims 31-38 are newly submitted (marked-up versions of the amended  
20 claims, showing additions and deletions, are included at the end of this document).

- 21 1. (Amended) An apparatus comprising:  
22 a substrate having first and second opposite edges;  
23 a plurality of memory devices disposed on the substrate;  
24 a plurality of channels extending between the opposite edges, wherein each  
25 of the plurality of memory devices is coupled to one of the plurality of channels;  
and

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01 FC:103  
02 FC:102

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168.00 CH  
LEE & HAYES, PLLC

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03 FC:116